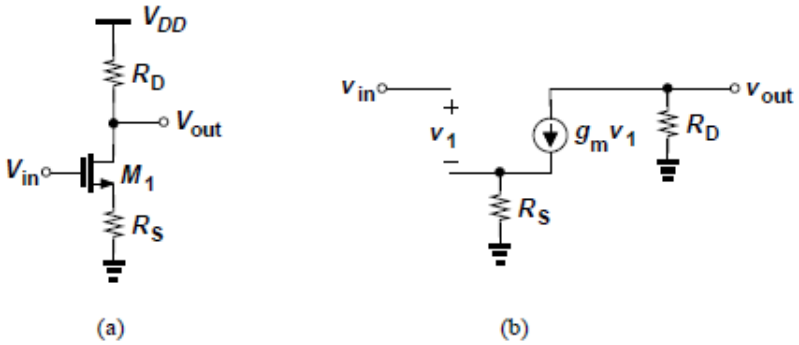


Figure 7.14 (a) CS stage with degeneration, (b) small-signal model.

Example 7.8

Compute the voltage gain of the circuit shown in Fig. 7.15(a) if $\lambda = 0$.

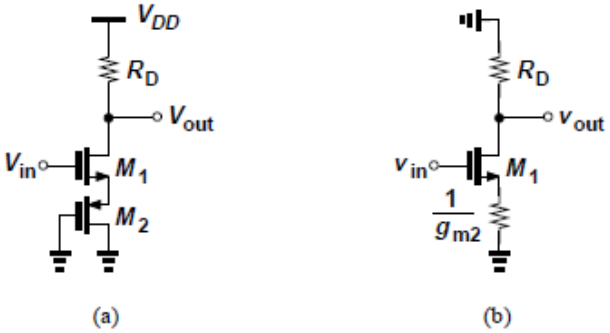


Figure 7.15 (a) Example of CS stage with degeneration, (b) simplified circuit.

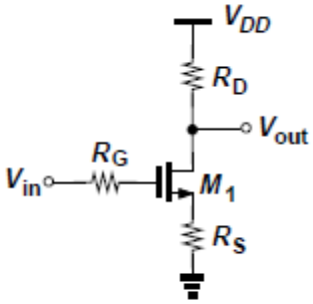


Figure 7.16 CS stage with gate resistance.

Example 7.9

Compute the output resistance of the circuit in Fig. 7.18(a) if M_1 and M_2 are identical.

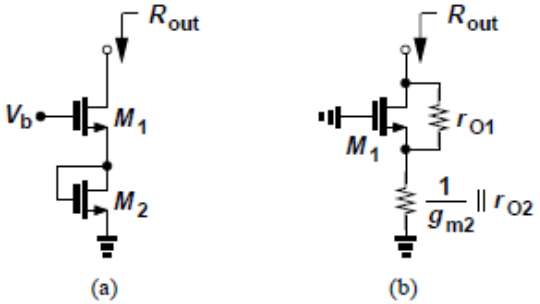


Figure 7.18 (a) Example of CS stage with degeneration, (b) simplified circuit.

Example 7.10

Determine the output resistance of the circuit in Fig. 7.19(a) and compare the result with that in the above example. Assume M_1 and M_2 are in saturation.

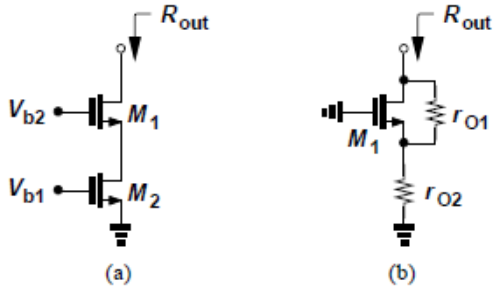


Figure 7.19 (a) Example of CS stage with degeneration, (b) simplified circuit.

Solution

With its gate-source voltage fixed, transistor M_2 operates as a current source, introducing a resistance of r_{O2} from the source of M_1 to ground [Fig. 7.19(b)].

Equation (7.71) can therefore be written as

$$R_{out} = (1 + g_{m1}r_{O1})r_{O2} + r_{O1} \tag{7.76}$$

$$\approx g_{m1}r_{O1}r_{O2} + r_{O1}. \tag{7.77}$$

Assuming $g_{m1}r_{O2} \gg 1$ (which is valid in practice), we have

$$R_{out} \approx g_{m1}r_{O1}r_{O2}. \tag{7.78}$$

7.2.5 CS Core With Biasing

The effect of the simple biasing network shown in Fig. 7.1 is similar to that analyzed for the bipolar stage in Chapter 5. Depicted in Fig. 7.20(a) along with an input coupling capacitor (assumed a short circuit), such a circuit no longer exhibits an infinite input impedance:

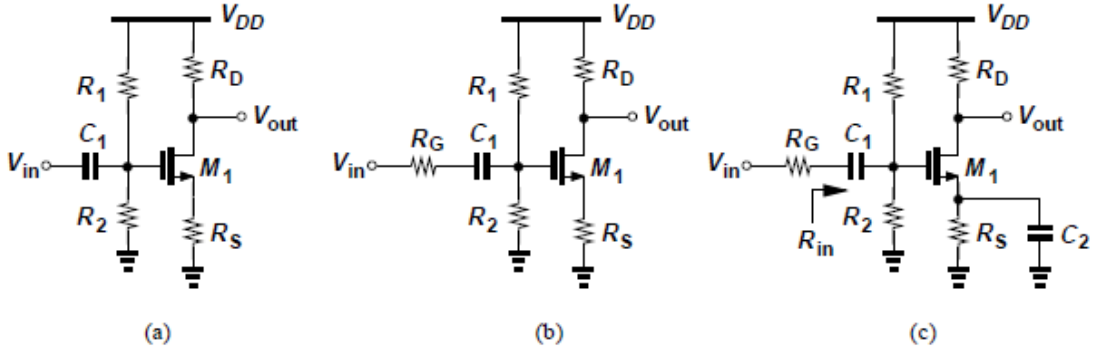


Figure 7.20 (a) CS stage with input coupling capacitor, (b) inclusion of gate resistance, (c) use of bypass capacitor.

$$R_{in} = R_1 || R_2. \tag{7.79}$$

Thus, if the circuit is driven by a finite source impedance [Fig. 7.20(b)], the voltage gain falls to

$$A_v = \frac{R_1 || R_2}{R_G + R_1 || R_2} \cdot \frac{-R_D}{\dfrac{1}{g_m} + R_S}, \tag{7.80}$$

7.3 Common-Gate Stage

Shown in Fig. 7.21, the CG topology resembles the common-base stage studied in Chapter 5. Here, if the input rises by a small value, ΔV, then the gate-source voltage of M_1 *decreases* by the same amount, thereby lowering the drain current by $g_m \Delta V$ and *raising* V_{out} by $g_m \Delta V R_D$. That is, the voltage gain is positive and equal to

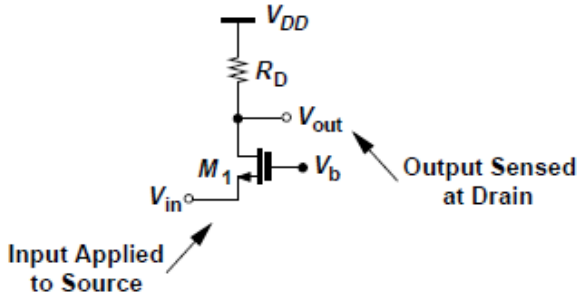


Figure 7.21 Common-gate stage.

$$A_v = g_m R_D. \tag{7.95}$$

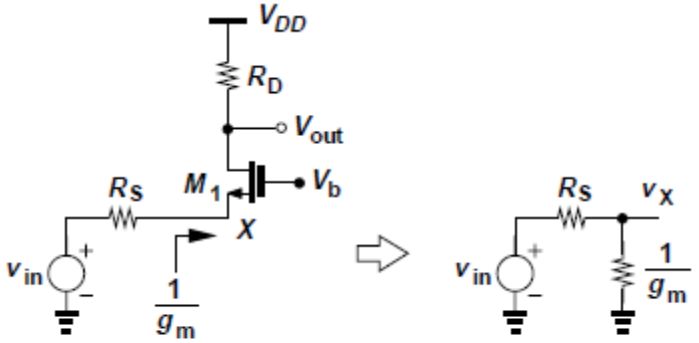


Figure 7.24 Simplification of CG stage with signal source resistance.

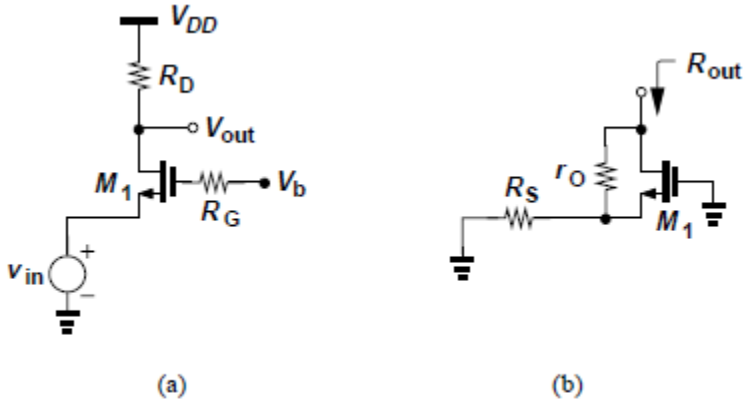


Figure 7.25 (a) CG stage with gate resistance, (b) output resistance of CG stage.

Example 7.13

For the circuit shown in Fig. 7.26(a), calculate the voltage gain if $\lambda = 0$ and the output impedance if $\lambda > 0$.

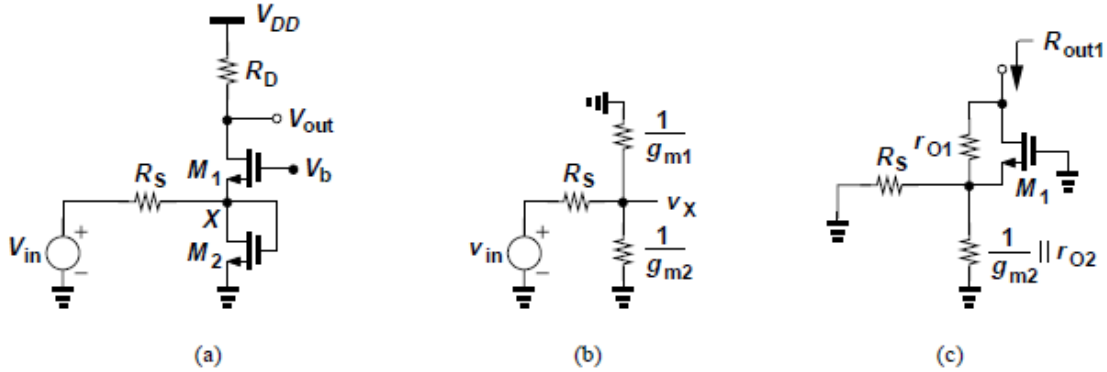


Figure 7.26 (a) Example of CG stage, (b) equivalent input network, (c) calculation of output resistance.

7.3.1 CG Stage With Biasing

Following our study of the CB biasing in Chapter 5, we surmise the CG amplifier can be biased as shown in Fig. 7.27. Providing a path for the bias current to ground, resistor R_3 lowers the input impedance—and hence the voltage gain—if the signal source exhibits a finite output impedance, R_S.

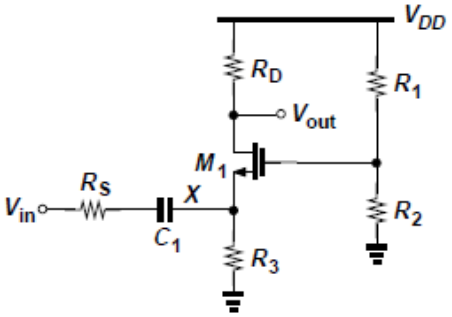


Figure 7.27 CG stage with biasing.

7.4 Source Follower

The MOS counterpart of the emitter follower is called the "source follower" (or the "common-drain" stage) and shown in Fig. 7.28. The amplifier senses the input at the gate and produces the output at the source, with the drain tied to V_{DD}. The circuit's behavior is similar to that of the bipolar counterpart.

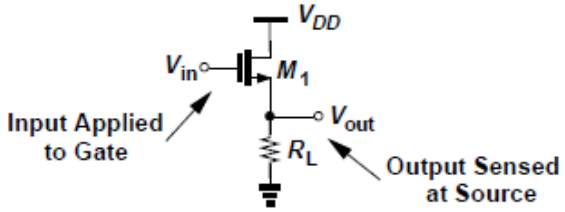


Figure 7.28 Source follower.

Example 7.16

A source follower is realized as shown in Fig. 7.30(a), where M_2 serves as a current source. Calculate the voltage gain of the circuit.

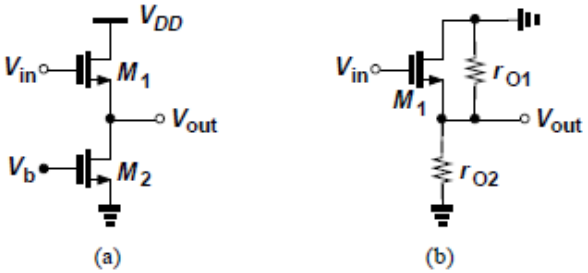


Figure 7.30 (a) Follower with ideal current source, (b) simplified circuit.

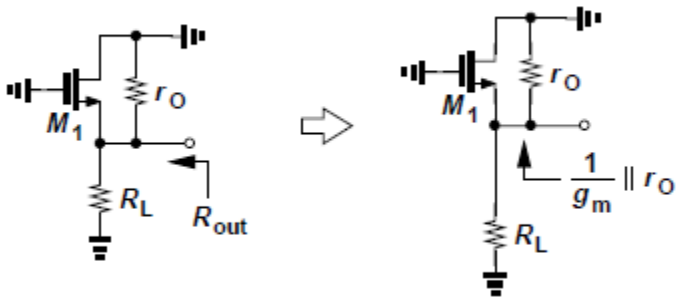


Figure 7.31 Output resistance of source follower.

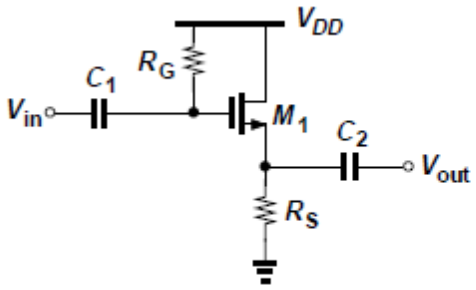


Figure 7.32 Source follower with input and output coupling capacitors.

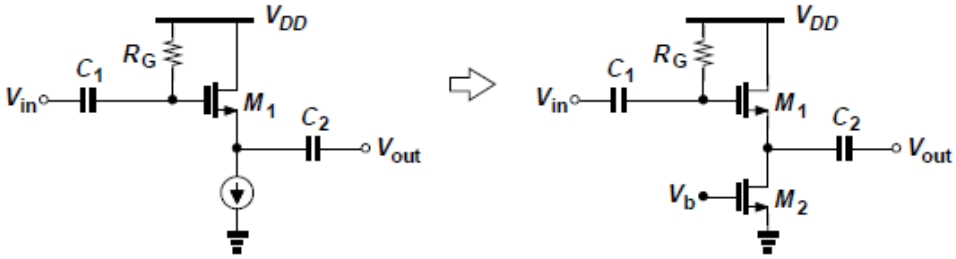


Figure 7.33 Source follower with biasing.

Example 7.19

Calculate the voltage gain and output impedance of the circuit shown in Fig. 7.34(a).

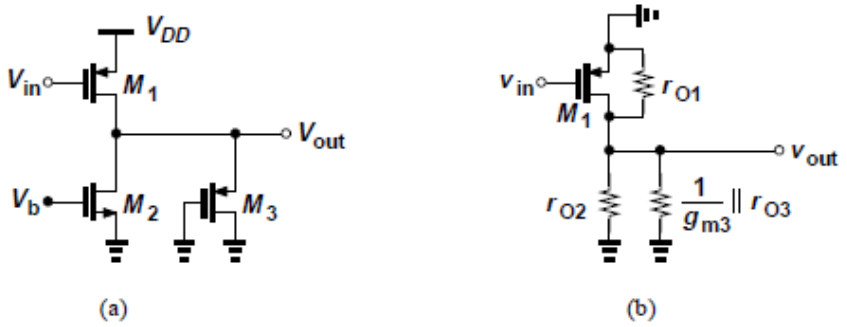


Figure 7.34 (a) Example of CS stage, (b) simplified circuit.

Example 7.20

Compute the voltage gain of the circuit shown in Fig. 7.35(a). Neglect channel-length modulation in M_1.

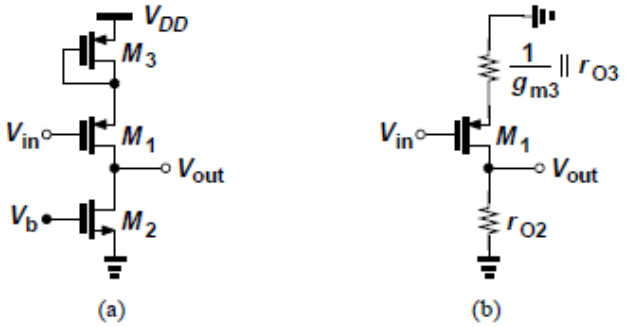


Figure 7.35 (a) Example of CS stage, (b) simplified circuit.

Example 7.21

Determine the voltage gain of the amplifiers illustrated in Fig. 7.36. For simplicity, assume $r_{O1} = \infty$ in Fig. 7.36(b).

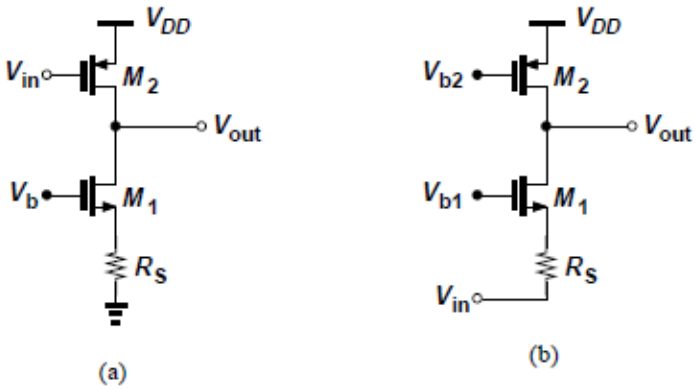


Figure 7.36 Examples of (a) CS and (b) CG stages .

Example 7.22

Calculate the voltage gain of the circuit shown in Fig. 7.37(a) if $\lambda = 0$.

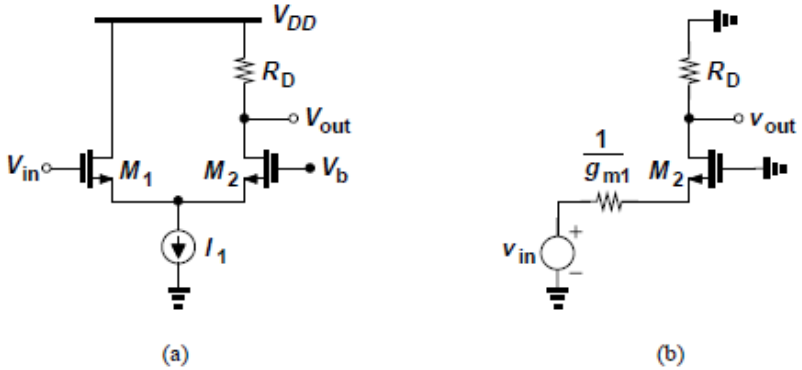


Figure 7.37 (a) Example of a composite stage, (b) simplified circuit.

Example 7.23

The circuit of Fig. 7.38 produces two outputs. Calculate the voltage gain from the input to Y and to X. Assume $\lambda = 0$ for M_1.

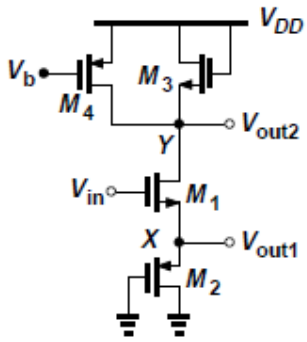
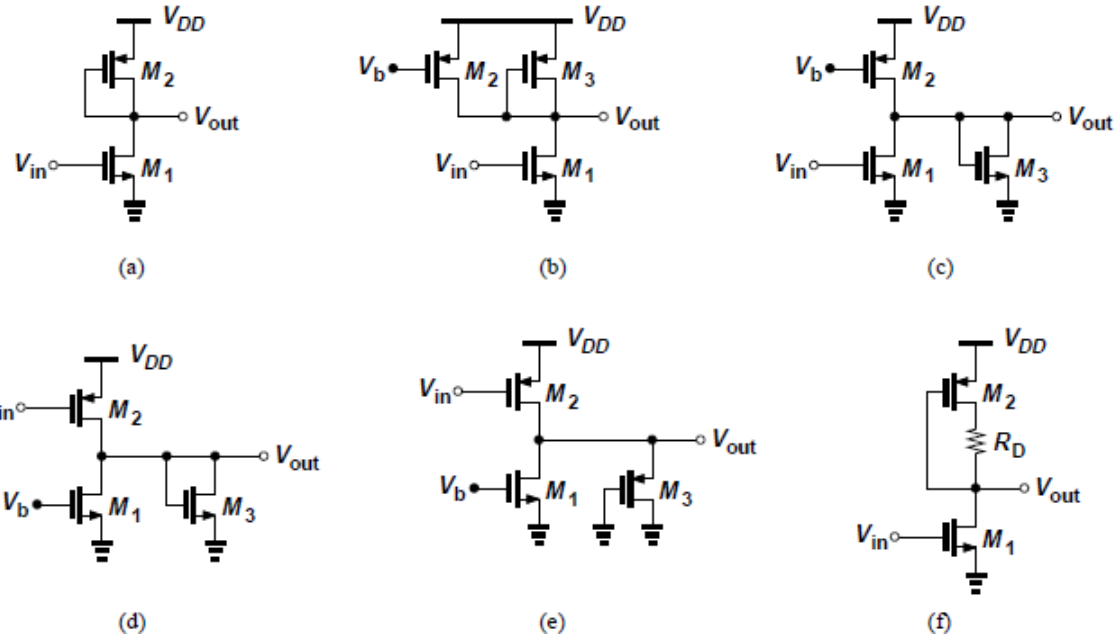


Figure 7.38 Example of composite stage.



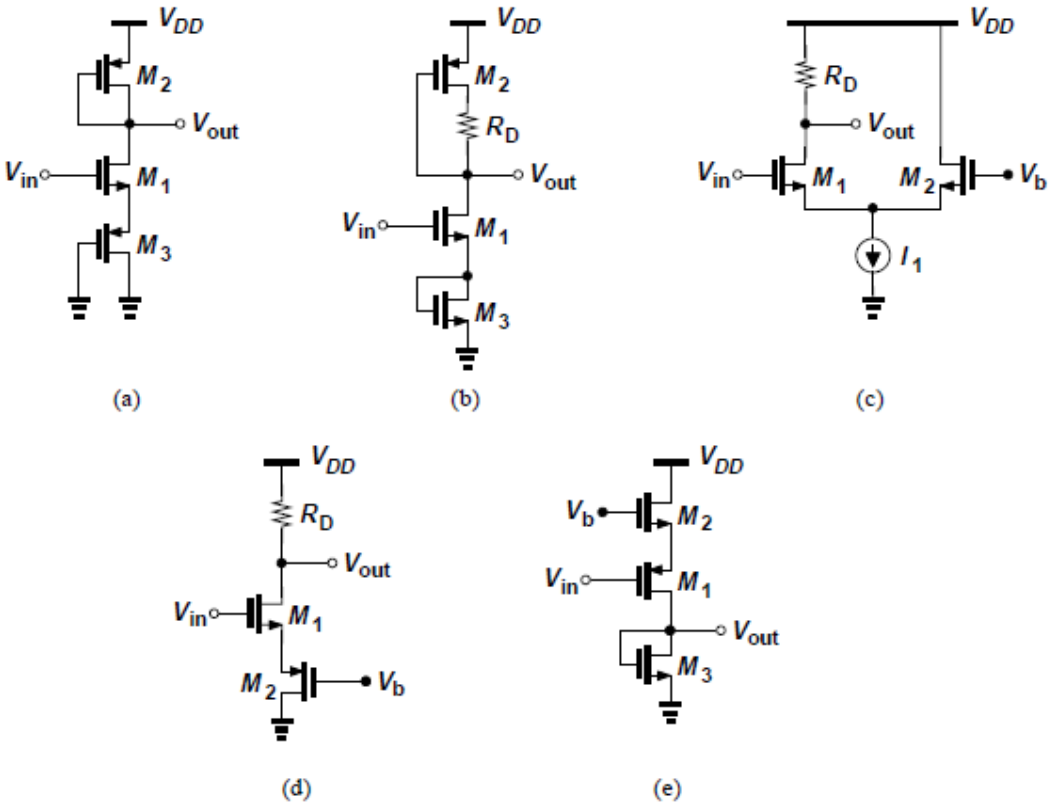


Figure 7.62

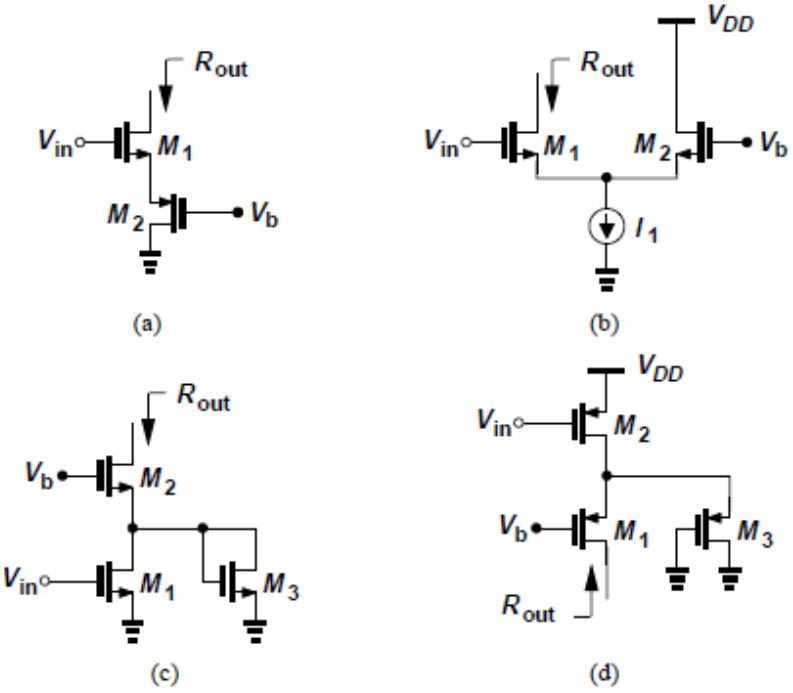


Figure 7.63

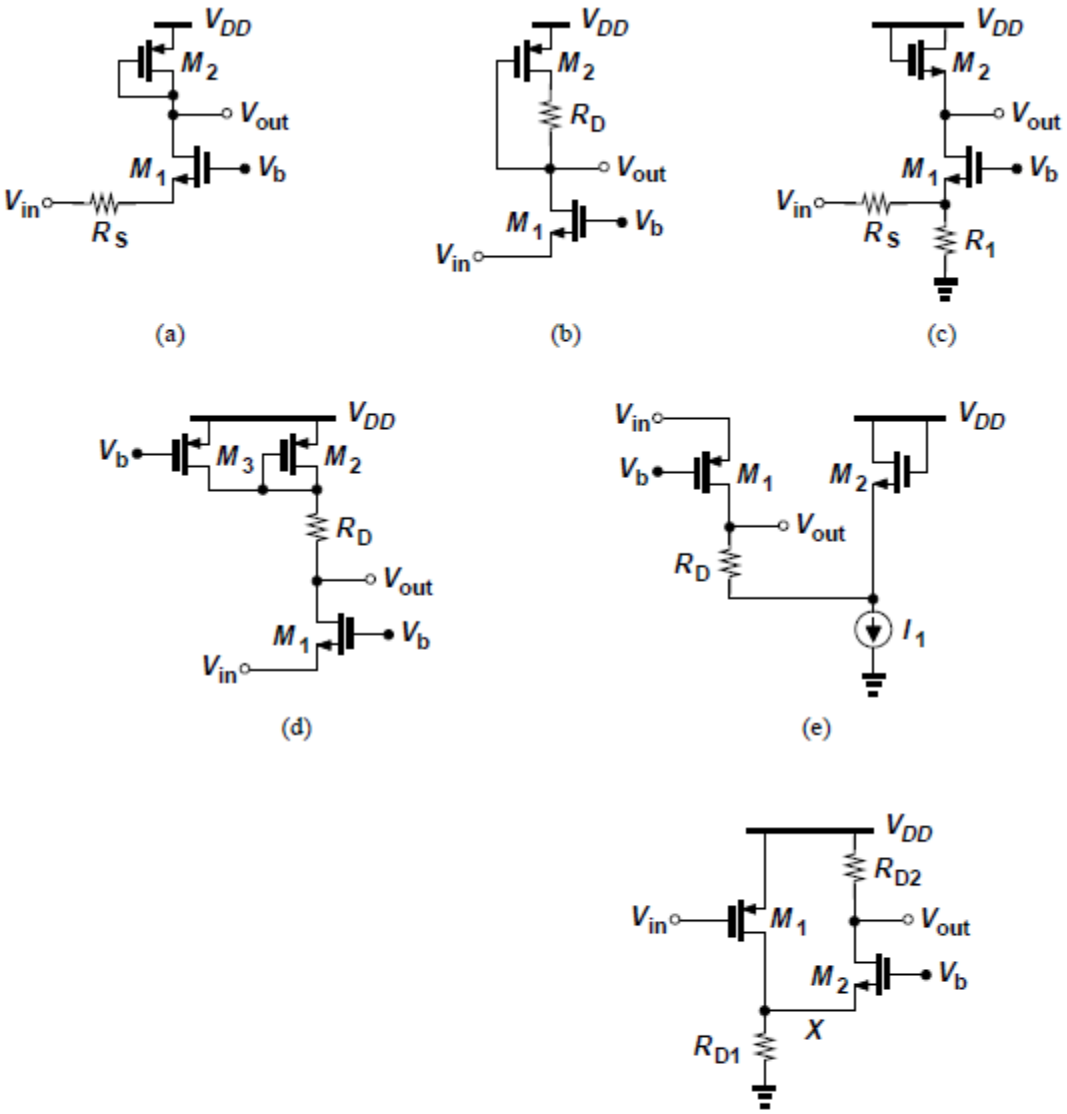


Figure 7.73

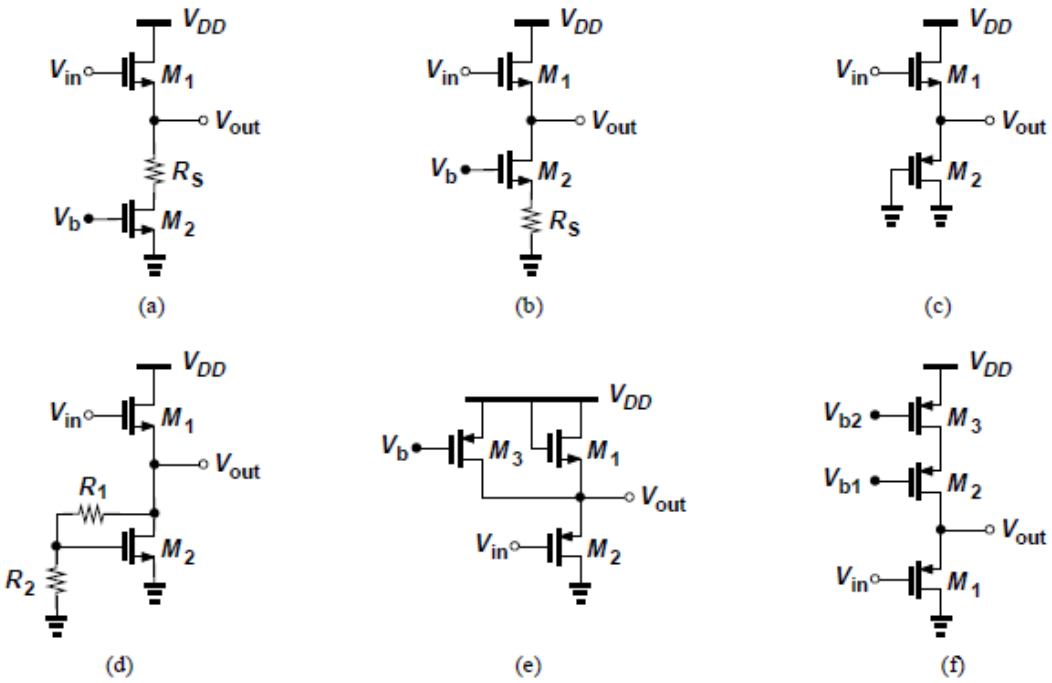


Figure 7.80

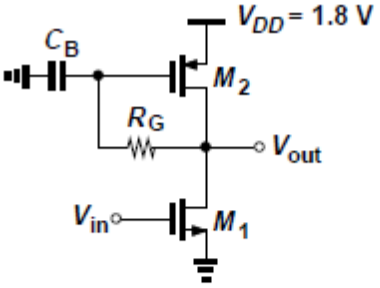


Figure 7.86

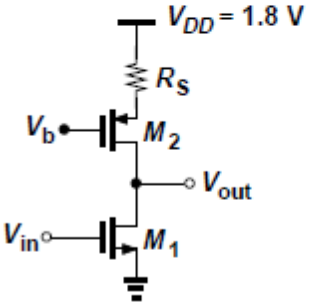


Figure 7.87

7.90, I_1 is an ideal current source equal to 1 mA.